ABSTRACT

A packaged semiconductor device (a wafer-level chip scale package) containing no UBM between a chip pad and an RDL pattern is described. As well, the device contains only a single non-polymeric insulation layer between the RDL pattern and the solder bump. The single non-polymeric insulation layer does not need high temperature curing processes and so does not induce thermal stresses into the device. As well, manufacturing costs are diminished by eliminating the UBM between the chip pad and the RDL pattern.